Amendments to the Specification

Please replace paragraph [0002] with the following amended paragraph:

Usually, a chip-size semiconductor package includes a Si chip; metal pads formed on the Si chip; a wafer coating formed over the Si chip; conductive wiring patterns formed on the wafer coating; a molding resin formed over the wafer coating; conductive posts formed in the molding resin; and terminals formed on the conductive posts ~~molding resin~~. The conductive wiring patterns are electrically connected to the metal pads through the wafer coating. The terminals are connected to the conductive posts one by one.

Please replace paragraph [0007] with the following amended paragraph:

According to a first aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; ~~a wafer coat formed over the semiconductor chip~~[[;]] a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~ electrically connected to the metal pad ~~conductive pattern~~; a molding resin formed over the conductive wiring pattern; ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[;]] and a terminal member which is electrically connected to the conductive wiring pattern, wherein the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion

and the extended portion. The ~~formed on the molding resin and is connected to the conductive post. A~~ connecting portion has a width that gradually decreases toward the extended portion, and the connecting portion has [[(]]~~boundary portion) of the conductive wiring pattern and conductive post is provided with~~ a slit to disperse stress to be applied to the connecting portion.

Please replace paragraph [0008] with the following amended paragraph:

Preferably, the connecting portion is provided with a plurality of slits, which are separated from each other. The slits may be shaped to be rectangular and arranged to extend radially. ~~Preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern~~[[.]]

Please replace paragraph [0009] with the following amended paragraph:

According to a second aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; ~~a wafer coat formed over the semiconductor chip~~[[;]] a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~ electrically connected to the metal pad ~~conductive pattern~~; a molding resin formed over the conductive wiring pattern; ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[;]] and a terminal member which is ~~formed on the molding resin and is connected to the conductive post~~[[;]] electrically connected to the

conductive wiring pattern, wherein the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion, the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and a dummy pattern arranged adjacent [[a]] the first and second boundaries and along sides of the connecting portion, the molding resin also being formed on the dummy pattern [[(]]~~boundary portion) of the conductive post and wiring pattern~~.

Please replace paragraph [0010] with the following amended paragraph:

Preferably, the dummy pattern is a conductive pattern which is formed in the same process as the conductive wiring pattern and is arranged parallel to the conductive wiring pattern. Further, the dummy pattern may include two parts arranged at [[the]] both [[side]] sides of the conductive pattern. ~~Further more, preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern, and~~ Furthermore, the two parts of the dummy pattern may be [[are]] arranged along the conductive post and conductive wiring pattern.

Please replace paragraph [0011] with the following amended paragraph:

According to a third aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor

chip; ~~a wafer coat formed over the semiconductor chip~~[[;] a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~ electrically connected to the metal pad ~~conductive pattern~~; a molding resin formed over the conductive wiring pattern; ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[;]] and a terminal member which is electrically connected to the conductive wiring pattern, wherein the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion, the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and ~~formed on the molding resin and is connected to the conductive post. At least one of the conductive wiring pattern and conductive post is provided with~~ a dent is formed at and around [[a]] the connecting portion [[(]]~~boundary portion) of the conductive wiring pattern and conductive post~~.

Please replace paragraph [0012] with the following amended paragraph:

The dent may be shaped to be square. ~~Preferably, the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern~~[[.]]

Please replace paragraph [0013] with the following amended paragraph:

According to a fourth aspect of the present invention, a chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; ~~a wafer coat formed over the semiconductor chip~~[[;]] a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~ electrically connected to the metal pad ~~conductive pattern~~; a molding resin formed over the conductive wiring pattern; ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[;]] and a terminal member which is electrically connected to the conductive wiring pattern, wherein the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion, the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and the connecting portion has ~~formed on the molding resin and is connected to the conductive post. The conductive wiring pattern is shaped to have~~ a first region extending outwardly from the terminal portion ~~conductive post~~ and a second region extending ~~vertically~~ from the ~~first region~~ connecting portion.

Please replace paragraph [0014] with the following amended paragraph:

Preferably, the second region comprises a plurality of projecting parts each of which extends vertically from the first region, and the projecting parts of the second

region are extended from both sides of the first region. ~~Further, the connecting portion may be shaped to decrease in area gradually from the conductive post to the conductive wiring pattern~~[[.]] At least one of the projecting parts may form a part of the ~~conductive post~~ connecting portion.

Please replace paragraph [0017] with the following amended paragraph:

For better understanding of the present invention, a conventional technology is first described in conjunction with Figs. 1 to 4. Fig. 1 is a cross-sectional view showing a conventional chip-size semiconductor package 10. Fig. 2 is a plan view showing the conventional chip-size semiconductor package 10, shown in Fig. 1. The chip-size semiconductor package 10 includes a Si chip 12; metal pads 14 formed on the Si chip 12; a wafer coating 16 formed over the Si chip 12; conductive wiring patterns 18 formed on the wafer coating 16 and including conductive portions 20A; a molding resin 24 formed over the wafer coating 16; conductive posts 20 formed in the molding resin 24 and on conductive portions 20A; and terminals 22 formed on the conductive posts 20A ~~molding resin 24~~. The conductive wiring patterns 18 are electrically connected to the metal pads 14 through the wafer coating 16. The terminals 22 are connected to the conductive posts 20 one by one.

Please replace paragraph [0018] with the following amended paragraph:

Fig. 3 is an enlarged view showing a part 30 encircled by a broken line in Fig. 2.

As shown in Fig. 3, a connecting portion (boundary portion) 40 between the conductive ~~post 20~~ portion 20A and wiring pattern 18 is extremely narrow and weak. According to the conventional chip-size package, the connecting portion 40 may be broken by stress, which is generated when the molding resin 24 is expanded or contracted.

Please replace paragraph [0019] with the following amended paragraph:

Fig. 4 is an enlarged view showing the part 30 of another conventional chip-size semiconductor package. As described above, a connecting portion (boundary portion) 140 is a part which is easily broken in response to stress, so that the connecting portion 140 is shaped to decrease in area gradually from the [[a]] conductive portion 120A ~~post 120~~ to a conductive wiring pattern 118.

Please replace paragraph [0020] with the following amended paragraph:

However, according to the chip-size semiconductor package, shown in Fig. 4, the area to be in contact with the molding resin 24 is increased, so that the molding resin 24 may be removed from the conductive portion 120A ~~post 120~~ and conductive wiring pattern 118. As a result, the connecting portion 140 may be broken easily.

Please replace paragraph [0022] with the following amended paragraph:

Fig. 5 is an enlarged view showing the part 30 of a chip-size semiconductor package according to a first preferred embodiment of the present invention. According

to the first preferred embodiment, a connecting portion (boundary portion) 240 of a conductive wiring pattern 218 and a conductive portion 220A are ~~post 220 is~~ provided with four slits 250 to disperse stress to be applied to the connecting portion 240. The connecting portion 240 is a part which is easily broken in response to stress, so that the connecting portion 240 is shaped to decrease in area gradually from the conductive portion 220A ~~post 220~~ to the conductive wiring pattern 218.

Please replace paragraph [0023] with the following amended paragraph:

The slits 250 are arranged to be separated by a predetermined distance from each other. The slits 250 are shaped to be rectangular and arranged to extend radially, as shown in Fig. 5. According to the first preferred embodiment, the slits 250 are provided, so that stress applied to the connecting portion 240 is dispersed, and the molding resin is well in contact or bonded with the conductive portion 220A ~~post 220~~ and conductive wiring pattern 218. As a result, the connecting portion 240 is not easily broken.

Please replace paragraph [0024] with the following amended paragraph:

Fig. 6. is an enlarged view showing the part 30 of a chip-size semiconductor package according to a second preferred embodiment of the present invention. According to the second preferred embodiment, dummy pattern 350 is formed around a connecting portion (boundary portion) 340 of a conductive wiring pattern 318 and a

conductive portion 320A ~~post 320~~. The dummy patterns 350 are arranged along the shape of the connecting portion 340. The connecting portion 340 is a part which is easily broken in response to stress, so that the connecting portion 340 is shaped to decrease in area gradually from the conductive portion 320A ~~post 320~~ to the conductive wiring pattern 318.

Please replace paragraph [0026] with the following amended paragraph:

According to the second preferred embodiment, the dummy patterns 350 are provided, so that stress applied to the connecting portion 340 is dispersed, and the molding resin is well in contact or bonded with the conductive portion 320A ~~post 320~~ and conductive wiring pattern 318. As a result, the connecting portion 340 is not easily broken.

Please replace paragraph [0027] with the following amended paragraph:

Fig. 7 is an enlarged view showing a part of a chip-size semiconductor package according to a third preferred embodiment of the present invention. Fig. 8 is a cross-sectional view taken on line A-A in Fig. 7. According to the third preferred embodiment, a dent 450 is formed around a connecting portion (boundary portion) 440 of a conductive wiring pattern 418 and a conductive portion 420A ~~post 420~~. The connecting portion 440 is a part which is easily broken in response to stress, so that the connecting portion 440 is shaped to decrease in area gradually from the conductive portion 420A

~~post 420~~ to the conductive wiring pattern 418. The dent 450 is shaped to be square.

Please replace paragraph [0028] with the following amended paragraph:

According to the third preferred embodiment, the dent 450 is formed around the connecting portion 440, so that stress applied to the connecting portion 440 is dispersed, and the molding resin is well in contact or bonded with the conductive portion 420A ~~post 420~~ and conductive wiring pattern 418. As a result, the connecting portion 440 is not easily broken.

Please replace paragraph [0029] with the following amended paragraph:

Fig. 9 is an enlarged view showing a part of a chip-size semiconductor package according to a fourth preferred embodiment of the present invention. According to the fourth preferred embodiment, a conductive wiring pattern 518 is shaped to have a first region 518a extending outwardly from a conductive portion 520A ~~post 520~~ and second regions 518b each of which is extending or projecting ~~vertically~~ perpendicularly from the first region 518a. The projecting parts of the second region 518b are extended from both sides of the first region 518a. One horizontal line of the projecting parts 518b forms a part of the conductive portion 520A ~~post 520~~.

Please replace paragraph [0030] with the following amended paragraph:

The connecting portion 540 is a part which is easily broken in response to stress,

so that the connecting portion 540 is shaped to decrease in area gradually from the conductive portion 520A ~~post 520~~ to the conductive wiring pattern 518.

Please replace paragraph [0031] with the following amended paragraph:

According to the fourth preferred embodiment, the conductive wiring pattern 518 is shaped to have the first region 518a and second regions 518b extending perpendicularly ~~vertically~~ from the first region 518a, so that stress applied to the connecting portion 540 is dispersed, and the molding resin is well in contact or bonded with the conductive portion 520A ~~post 520~~ and conductive wiring pattern 518. As a result, the connecting portion 540 is not easily broken.

Please replace the abstract with the following amended abstract:

A chip-size semiconductor package includes a semiconductor chip; a metal pad formed on the semiconductor chip; ~~a wafer coat formed over the semiconductor chip~~[[;]] a conductive wiring pattern ~~formed on the wafer coat, in which the metal pad is~~ electrically connected to the metal pad ~~conductive pattern~~; a molding resin formed over the conductive wiring pattern; ~~a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern~~[[;]] and a terminal member which is ~~formed on the molding resin and is connected to the conductive post. A~~ electrically connected to the conductive wiring pattern, wherein the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion. The connecting portion [[(]]~~boundary portion) of~~ between the extended portion and the terminal portion ~~conductive wiring pattern and conductive post~~ is provided with a slit, to disperse stress [[to be]] applied to the connecting portion.